# Specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
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</table>
| **Processor** | Xilinx Zynq-7020 System on Chip (SOC)  
Dual Arm Core and Reconfigurable 7-Series FPGA Fabric  
2.5 DMIPS/MHz per CPU  
CPU frequency: 766 MHz |
| **IO** |  
**Reconfigurable IO:**  
26x MIO (Multiplexed IO)  
60x HR SelectIO (High Range Select IO)  
*Not all interfaces can be used simultaneously* |
| **Memory** | 32 Gbit Rad Tolerant NAND Flash [FM]  
2 Gbit NAND Flash [EM]**  
8 Gbit DDR3 SDRAM (4 Gbit when EDAC is active) *** |
| **FPGA Programmable Logic** |  
10 MHz — 250 MHz Clock  
24 differential pairs, 12 single ended  
140 – 36Kbit Block RAM (4.9 Mbit)  
Programmable I/O Blocks Support LVCMOS, LVDS, and SSTL, with 1.8 V, 2.5 V, 3.3 V I/O |
| **Power** | 1.6 W — 2.85 W |
| **Size** | Designed in a 1U Cubesat form factor (8.81 cm x 8.95 cm)  
Thickness: 0.25 cm (tallest component) [EM]  
Thickness: 1.73 cm (tallest component) [FM] |
| **Mass** | 60 g [EM]  
74 g [FM] |

*Legacy Note: All CSP EMs in the 94500 and 97930 RevE series and prior are manufactured with 8 Gbits of NAND Flash.*  
**Legacy Note: All CSP EMs in the 94500 and 97930 RevJ series and prior are manufactured with 2 Gbits of SDRAM.*
## Interfaces

### CSP Evaluation Board
- **EM kit includes:**
  - Connects to Samtec SEAF-RA 4x40 Connector on CSP
- **Included PHYs:**
  - 1x USB
  - 1x Ethernet
  - 1x JTAG
  - 1x UART
  - 3x SpaceWire
  - 1x CameraLink
- **GPIO Breakout Headers**
- **Power Regulators to Power CSP**
- **FMC Header**

### CSP USB/UART Board
- **Connects to Evaluation Board**
- **USB to UART Converter**
- **RS-422 Converter**

### CSP Board
- **SpaceWire**
- **UART**
- **SPI**
- **I2C**
- **JTAG**
- **Ethernet**
- **USB**

*Requires external PHY (Included with EM Evaluation Board)

## Specifications

### Parts Grade
- **Commercial Space**

### Operating Temperature
- **CSP-01:** EM 0°C to 70°C
- **CSP-02:** FM 0°C to 70°C

### Workmanship Standards
- **CSP-01:** IPC-A-610 Class 2 Acceptability of Electronic Assemblies
- **CSP-02:** IPC-A-610 Class 3 Acceptability of Electronic Assemblies, J-STD-001 with the J-STD-001 Space Addendum

### End Item Data Package (EIDP)

#### Engineering Model
- CSP PCBA Kit Test Procedure/Record
- CAD Model for CSP PCBA (SolidWorks)
- Certificate of Conformance

#### Flight Model
- CSP Board Test Procedure/Record
- CSP Load Procedure/Record
- Random Vibration Test Procedure/Record
- Thermal Cycle Test/Record
- Burn-In Test Procedure/Record
- Non-Environmental Test Procedure/Record
- Certificate of Conformance
Specifications

Hardware Models
CSP-01: Engineering Model [EM]
CSP-02: Flight Model [FM]

Connector
Samtec SEAF-RA 4x40 Connector
Designed to be Connected to a Samtec SEAM 4 x 40 Backplane

Radiation Tolerance

<table>
<thead>
<tr>
<th>SEL</th>
<th>No Destructive Events</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEE</td>
<td>Unmitigated—Same SEE rates as a commercial Xilinx 7 family Zynq part</td>
</tr>
<tr>
<td>TID</td>
<td>30 krads (Si)</td>
</tr>
<tr>
<td>SEFI</td>
<td>Mitigated with Watchdog for ARM Cores (Patent Number 7,237,148 plus Re-Examination Certificate number RE42,314 C1)</td>
</tr>
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Software

Operating Systems
Bare Metal
- Bare-metal functional test code is included.
Linux
- Buildroot configuration files are provided to support Linux development.
ThreadX
- Supported with additional license purchase—contact factory for more information

Many additional Options are supported on the Zynq-7020. Refer to Xilinx literature for more details.

Testing

<table>
<thead>
<tr>
<th>Tested Interfaces (EM and FM)</th>
<th>Test Code Provided</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAND Flash</td>
<td>Yes</td>
<td>Tested across entire memory range.</td>
</tr>
<tr>
<td>DDR3/SDRAM</td>
<td>Yes</td>
<td>Tested across entire memory range. Read and write eye tested.</td>
</tr>
<tr>
<td>SpaceWire*</td>
<td>Yes</td>
<td>Transmit (Tx) and Receive (Rx) packets validated through external SpaceWire probe.</td>
</tr>
<tr>
<td>Ethernet PHY*</td>
<td>Yes</td>
<td>Internet ping test. Assigned MAC address.</td>
</tr>
<tr>
<td>USB-UART</td>
<td>Yes</td>
<td>Tx and Rx packets used for outputting all serial test data to external PC.</td>
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*Only tested in default configuration.*
Figure 1: CSP-02 FM (dimensions in inches)

Figure 2: CSP-01 EM on Evaluation Board

Figure 3: CSP-01 EM Development Kit

CSP Development Kit
1. Evaluation Board
2. USB to UART Converter Board
3. CSP