Space Micro offers a reconfigurable Image Processing Computer (IPC-7000™) containing user programmable Field Programmable Gate Arrays (FPGAs) and Digital Signal Processors (DSP), plus an embedded Solid State Buffer (SSB) memory. The IPC Product offers multiple camera inputs at >4 Gbps aggregate input rate, two reconfigurable FPGAs with local SDRAM and SRAM memories, plus DSP processing. An internal 64Gb SSB memory can be used for storage until download to a downlink Satellite.

Space Micro's IPC product line includes DSP based radiation hardened Single Board Computers. The ProtonX-Box impressive modularity supports low mission requirements, with the Proton2X-Box targeted for higher performance applications. All of our Digital products feature scalable parts programs up to full NASA level 1/Military Class S.

The IPC image processing computer is typically provided in a three board set that combines very high speed reconfigurable processing, low power radiation hardened computing and high-speed mass memory to meet the challenges of space imaging environments. The IPC is provided with Virtex 7 FPGAs (IPC-7000) and provides reconfigurable FPGA computing with two digital signal processors and an internal >2 Gbps bus to provide real-time image processing and storage of complex image streams. The IPC can also be reconfigured to provide in-flight firmware changes, allowing users to modify performance.

**FEATURES**

- Flight heritage on ORS-1 (>35,000 hours), delivered to other DoD programs
- In production on multiple flight missions
- Compact 3-board set
- Interface options include high-speed fiber optic and LVDS
- Algorithms-customer hosted and Space Micro provided
- Real-time 12 bit JPEG compression
- Patented TTMR and H-Core radiation mitigation techniques
**Single Board Computer (SBC) Features:**
- Floating point DSP - 900 MFLOPS at 1E-4 unrecoverable errors/day
- 128 MB EDAC protected RAM
- 4 Gb rad hard flash memory
- Programmable speed UARTs
- 1 Mbps synchronous serial ports
- Variable power control

**Solid State Buffer Features:**
- 256 GB per slice
- Number of slices customizable to meet memory requirement
- Optional EDAC

**Image Processing (IPC) Features:**
- Dual Fibre optic input > 1 Gbps
- Virtex 7 FPGA Processing with Reconfigurable bitmaps
- Local RAM buffering
- 128 MB EDAC protected RAM
- 4 Gb rad hard flash
- Fibre optically coupled or LVDS IF

**Customer Programmable Embedded Image Processing:**
- Customer Programmable FPGAs or SMI option, including:
  - Real-time 12 bit JPEG compression
  - Real-time non-uniformity correction
  - Multiple image channels
  - Channel formatting and packetization

**Radiation:**
- >100 krads (Si) total dose tolerance
- Single Event Latchup (SEL) Immune >70 MeV/μg/cm²
- No SEFI
- SEU tolerance 1E-4 unrecoverable errors/day

**Power:**
- 40 watts (depending upon peripherals, speed)

**Software Development Kit (SDK):**
- Texas Instrument software development tool support chain for SBC and IPC processors, with TI’s “DSP BIOS” real-time operating system
- Xilinx Virtex 7 FPGA development tools
- Board Support Package (BSP)