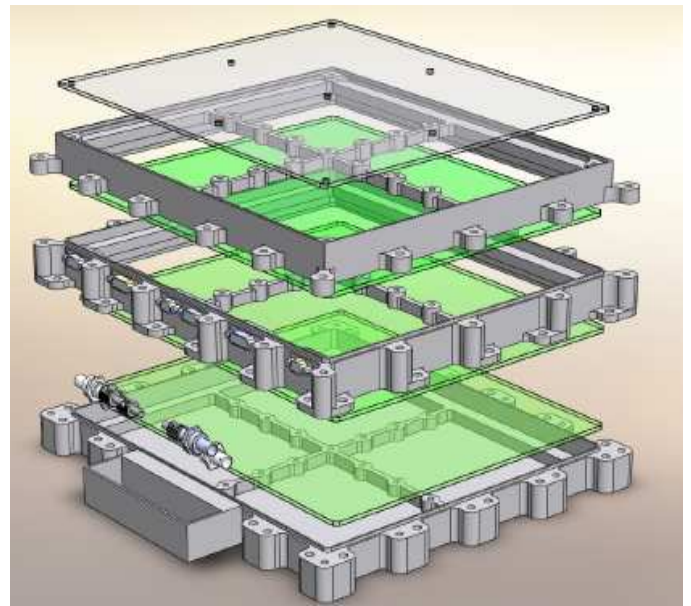


IPC5000™ Image Processing Computer



Gigahertz Speed Image Processing with Solid State Storage

High-performance processing, Mass Memory and Radiation Hardened. Our solutions continue to narrow the gap between state-of-art commercial and radiation-hardened satellite computing platforms. Space Micro's industry leading solutions for single event and total dose radiation effects provide extraordinary performance benefits by removing the barriers associated with using commercial processing in space. The IPC5000™ radiation-hardened image processing computer provides very high-speed, reconfigurable processing and mass memory storage, along with Space Micro's radiation effects mitigation techniques, to link between high-speed imagers and download communication platforms.

Space Micro Inc

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IPC5000™ Image Processing Computer

The IPC5000™ image processing platform is a three board set that combines high performance, low power radiation hardened computing and high-speed mass memory to meet the challenges of the space imaging environments. By utilizing Space Micro's patent pending radiation hardening technologies, Space Micro provides reconfigurable FPGA computing with two digital signal processors and an internal >2 Gbps bus to provide real-time image processing and storage of complex image streams. Space Micro, using its patent-pending Time-Triple Modular Redundancy™ (TTMR™), and Hardened Core (H-Core™) technologies has proven to solve the SEU/SEFI issues often seen in DSPs and reconfigurable FPGAs, enabling these capabilities. The IPC5000 is available with 12 bit JPEG compression and data/image formatting, or can be configured by the customer for specific applications.

FEATURES:

- Three board set:
 - SBC controller & bus interface
 - Solid State Buffer
 - Image Processing Computer
 - Fully radiation hard boards
- Single Board Computer (SBC) features:
 - Floating point DSP - 900 MFLOPS at 1E-4 unrecoverable errors/day
 - 128 MB EDAC protected RAM
 - 4 Gbit rad hard flash memory
 - Programmable speed UARTs
 - 1 Mbps synchronous serial ports
 - Variable power control of IPC5000
 - Low power 10W operation
- Solid State Buffer Features:
 - 64 Gbit high-speed SDRAM
 - 2 Gbps+ input data rate
 - Optional EDAC
 - Low power 6.5W operation
- Image Processing Computer (IPC) features:
 - Dual input fibre optic input
 - >1 Gbps
 - Rad hard Virtex 5 FPGA processing
 - Reconfigurable bitmaps
 - Local RAM buffering
 - 128 MB EDAC protected RAM
 - 4 Gbit rad hard flash
 - Gigabit Ethernet download output
- Fibre optically coupled IF
- LVDS option available
- Embedded, image processing
 - Real-time 12 bit JPEG compression
 - Real-time non-uniformity correction
 - Multiple image channels
 - Channel formatting and packetization
- Radiation Hardened
 - >100 krad (Si) total dose tolerance
 - Single Event Latchup (SEL) Immune >70 MeV/mg/cm2
 - No SEFI
 - SEU tolerance 1E-4 unrecoverable errors/day
- Power: 40 watts worst case configuration (depending upon peripherals, speed)
 - Low power operation 7W
- Compact slice form factor

SOFTWARE DEVELOPMENT KIT (SDK):

- Texas Instrument software development tool support chain for SBC and IPC processors, with TI's "DSP BIOS" real-time operating system
- Xilinx Virtex 5 FPGA development tools
- Board Support Package (BSP)

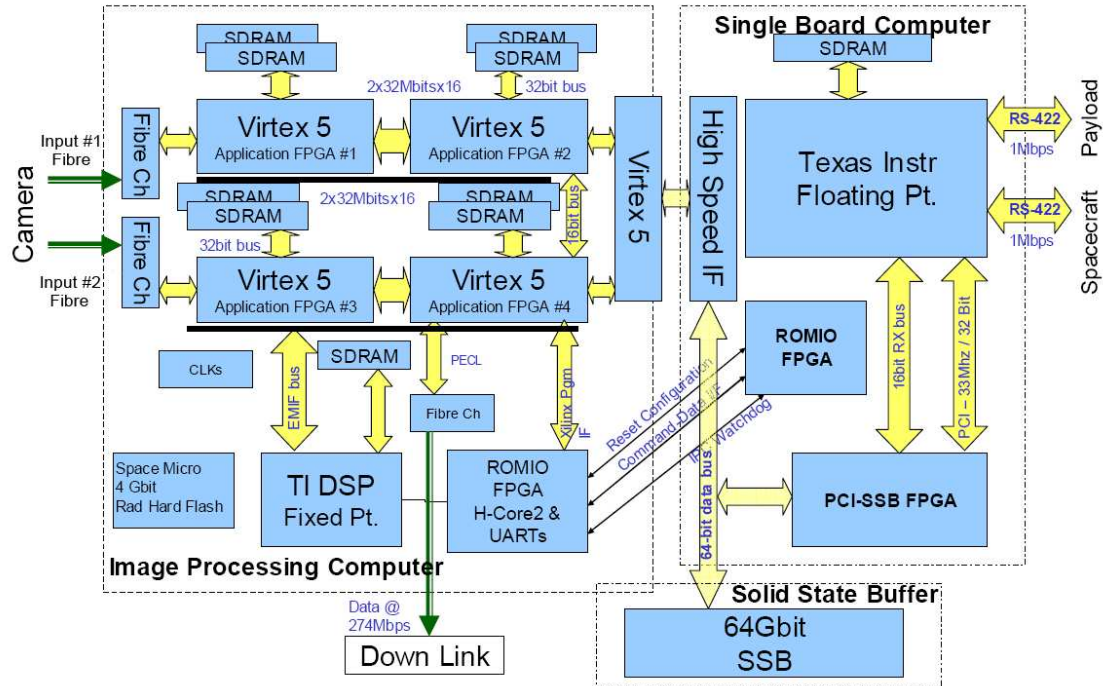
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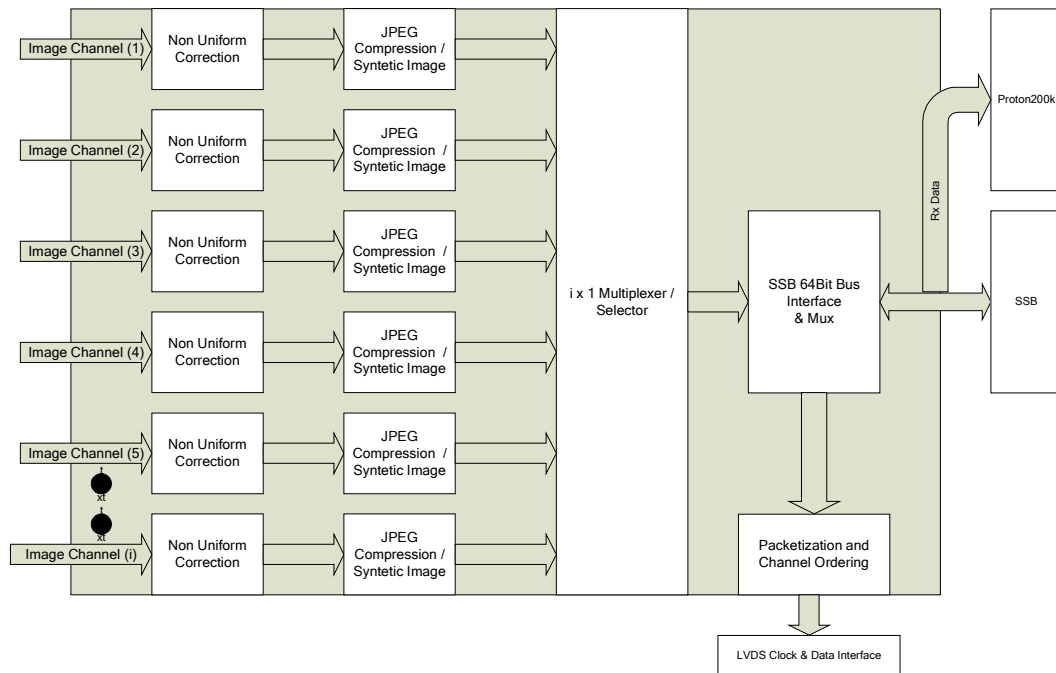


IPC5000™ Image Processing Computer

IPC5000 System Block Diagram (3 Boards)



IPC5000 Algorithm Flow



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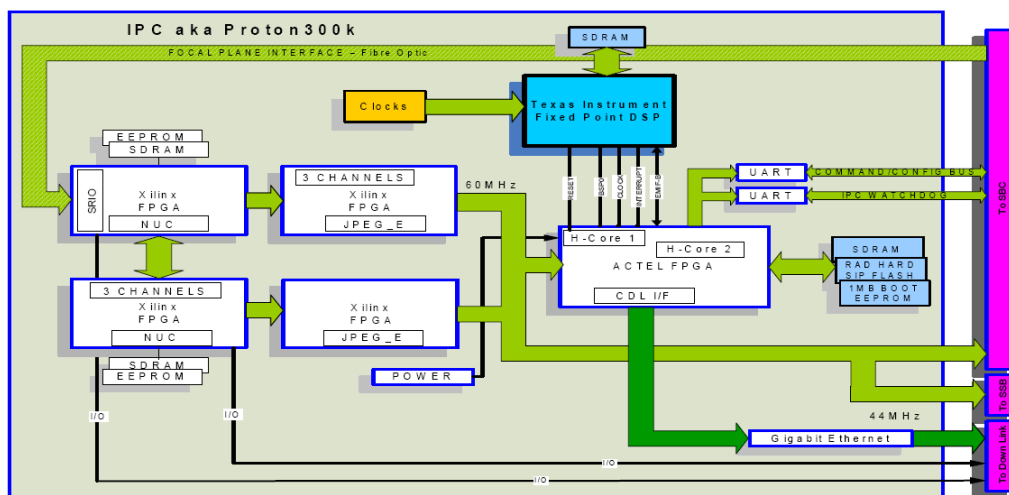
IPC5000™ Image Processing Computer

User Selectable Compression Ratios



The IPC5000™ image processing computer platform can be reconfigured to provide in-flight firmware changes. Additionally, up to 30 bitmaps can be stored in the local radiation hardened flash memory array. This allows users to develop systems quickly and modify performance in-flight. The IPC5000™ has flight heritage on Air Force missions and is ideal for a variety of different imaging applications.

Image Processing Computer (IPC) Block Diagram



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