

Proton Testing of SEFI Mitigation Technique for Microprocessors

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35-Word Abstract:

We describe a single event functional interrupt (SEFI) mitigation technique that monitors and maintains the operational status of commercial microprocessors in radiation environments. Proton radiation test results using this technique with an Intel Pentium III microprocessor are presented.

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1 Introduction

The use of leading-edge commercial microprocessors in space applications is precluded primarily due to their susceptibility to single-event upsets (SEU) and single-event functional interrupts (SEFI). The SEU and SEFI threshold LETs for commercial microprocessors can range from 0.2 to 9 MeV-cm²/mg[1]. In orbit environments, these thresholds translate to upset rates ranging from a few upsets per day (unacceptable) to a single upset per year (acceptable).

SEFIs are observed in complex integrated circuits and microprocessors as unexpected “hangs” during normal operation of the component. Such interruptions are believed to be due to single-event upsets in critical regions (such as a state machine) that force the circuit to an invalid state. Swift *et al.*[2] have advised space designers that SEFI is an emerging radiation hardness assurance issue with the solution cited as “removal of power supply and subsequent re-initialization.” This is currently the most common method of recovering from SEFI events in microprocessors. While a very safe solution, this procedure can be time consuming and result in severe design and operation consequences.

In this paper we present a SEFI mitigation technique that is capable of restoring the normal operation of an affected microprocessor without requiring the removal of power supply. This technique utilizes a sequence of signals with escalating levels of severity to drive the microprocessor out of its non-operational state to a known valid state. The use of a sequence of signals allows one to revive the microprocessor using the least severe technique possible so that normal operation can be restored faster. After entering a valid state the microprocessor can restore its normal operation without cycling power to the enclosing system. This technique has been used to restore the operation of an Intel Pentium III processor under proton irradiation after SEFI events. The results presented here show that the microprocessor could be restored to normal operation after every SEFI event without requiring the removal of power supply.

2 SEFI Mitigation Technique

The mitigation technique presented here uses an external circuit, called the “SEFI Hardened Core” (H-Core), to monitor and manage a COTS microprocessor (CPU) during SEFI events. The H-Core is responsible for detecting the occurrence of SEFI events and, in case of such an event, asserting a sequence of signals until complete recovery of the microprocessor is confirmed. In addition, the H-Core also provides capabilities for application programs to restore their states after recovery from a SEFI event.

The H-Core monitors the CPU by sending it a periodic low duty-cycle query signal. The CPU is required to send the correct “answer” to this signal within a preset period of time. If the H-Core does not receive an answer within this period, it assumes that the CPU has failed either due to a SEFI event or a non-SEFI event such as a failed application software. At this stage, the H-Core starts sending a sequence of signals to the CPU in order to force it to enter a valid state. After sending each signal, the H-Core expects the CPU to respond if it has recovered. If the CPU does not respond, the H-Core continues to send signals with escalating levels of severity. A higher level of severity implies that it may take longer for the CPU and the application programs to restore their states. If the CPU recovers in response to one of the signals, the application programs restore their states and continue execution while the H-Core reverts back to monitoring the processor. If the CPU does not recover in response to any of the above signals, the H-Core can trigger an external circuit to cycle the power to the entire computer system. As shown in Section 4, during our tests we were able to recover the CPU after all SEFI events without cycling the power to the test computer. The signals used by the H-Core in order to revive the CPU include:

- Available CPU-specific interrupts asserted in predetermined order.
- Local APIC watchdog signal(s) if available on the processor.
- Software reboot through a software watchdog.
- Hardware reset using the CPU's RESET pin.

In addition, the H-Core contains a signal line that is asserted while it is attempting to recover the CPU. This line is used by the recovery routines to check if the CPU has been in a SEFI state. The H-Core

circuit itself can be prevented from radiation-induced failures by using either triple modular redundant FPGAs or radiation-hardened ASICs.

3 Experimental Setup and Test Procedure

An 850MHz Intel Pentium III microprocessor was selected as a test device during our experiments. The Intel Pentium III (PIII) series processors have a well-known sensitivity to protons and, in particular, are known to be susceptible to SEFI[3]. The PIII processor was used with a VSBC-8d single-board computer by Versallogic Inc. The VSBC-8d test computer provides a VGA output, a serial port, an ethernet port, and an IDE interface. The test computer operated using GNU/Linux operating system installed on a hard drive.

During the radiation experiments, the VSBC-8d test computer was controlled and monitored using a separate monitor computer running Microsoft Windows 2000. The monitor computer was placed approximately 60 feet from the test computer during the experiments. The monitor computer and the

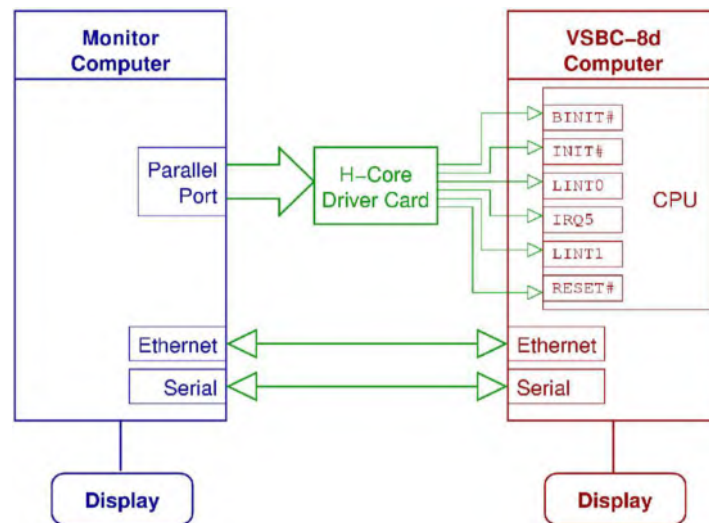


Figure 1 Major hardware components of the SEFI test setup.

test computer were connected together using their ethernet interfaces (Figure 1). This ethernet-based network was used for remote login and monitoring of the test computer during the radiation experiment. In addition, the console output of the test computer was also monitored by connecting the two computers through their serial ports. In order to achieve complete manual control of the H-Core signals, the H-Core circuit board was controlled using the parallel port of the monitor computer.

After reviewing the datasheet of the PIII processor[4], the H-Core was designed to assert the following signals (in increasing level of severity): BINIT#, INIT#, LINT0, IRQ5, LINT1/NMI, and RESET#. The VSBC-8d computer also contains a hardware watchdog timer that can be used to reset the computer in case of a hang. This watchdog was used in a subset of experiments to revive the processor after SEFI events. In addition, a software watchdog supported by the GNU/Linux operating system was also utilized in a subset of experiments to perform a software reboot in case of SEFI events. Similarly, in a subset of experiments, the local APIC timer was used as a watchdog to generate the LINT1/NMI signal in case the processor stopped responding.

The proton irradiation experiments were performed at the Crocker Nuclear Laboratory (CNL) of the University of California, Davis. The Radiation Effects Facility at CNL is based on a 76" isochronous cyclotron. The facility provides proton, deuteron, and He-4 (alpha particle) beams upto energies of 68, 45, and 90MeV, respectively. In our experiments, the PIII chip was irradiated with a focused beam with 51MeV protons at room temperature. No other components of the VSBC-8d computer were exposed to irradiation.

The operation of the test computer was monitored by continuously running a set of test routines that

activate various sections of the PIII processor. All test routines were recorded and monitored from the monitor computer during proton irradiation. The processor was assumed to have suffered a SEFI event when the above test loop was unexpectedly interrupted and the VSBC-8d computer stopped communicating with the monitor computer. At this stage, the monitor computer was used to assert the various H-Core signals to the test processor. The interrupt service routines of the processor were setup to provide a pre-determined set of responses to the H-Core signals. A signal was said to be successful if it resulted in a valid response from the processor.

4 Results

In order to verify the response of the test processor to H-Core signals, five calibration experiments were performed without any radiation exposure. During these calibration experiments, various H-Core signals were asserted from the monitor computer and the response of the test computer monitored. The test computer yielded the correct response to all H-Core signals during these calibration sequences.

After the calibration experiments, we performed twenty-one (21) SEFI experiments where the test processor was irradiated using the proton beam. In all of these cases, the processor suffered a SEFI event and stopped responding. In addition, we were able to recover normal operation of the processor in all cases using the H-Core signals without cycling the power to the test computer. The same PIII processor was used in all twenty-one SEFI test sequences. The total radiation dose exposure of the test processor was 625 rad(Si) which is well below the reported survivability of over 85 krad(Si) [3].

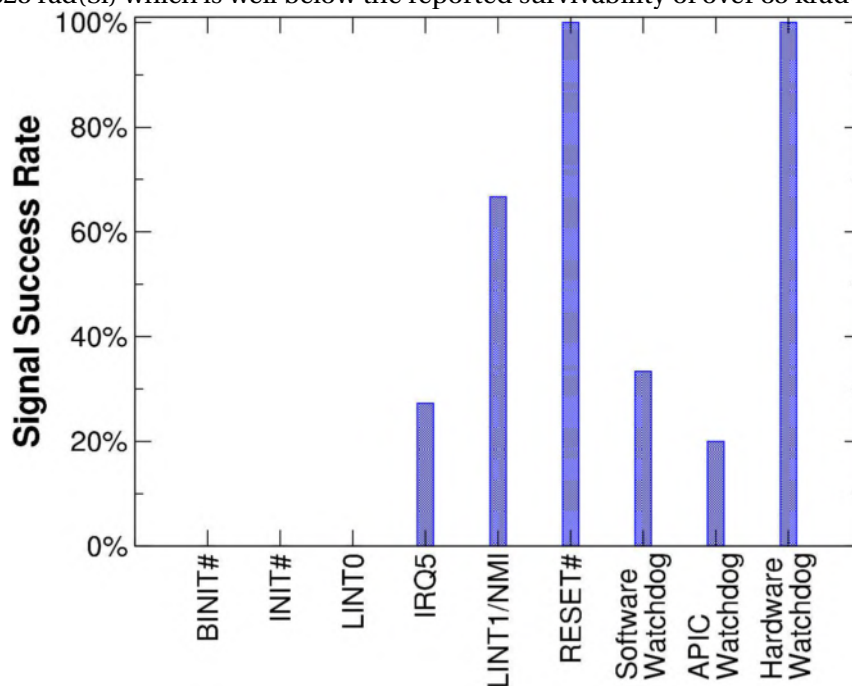


Figure 2 Success rates of various H-Core signals used with the PIII test processor after SEFI events.

The success rate of each of the H-Core signals was also recorded during the experiments and is summarized in Figure 2. The BINIT# signal resets the bus state machines while the INIT# signal resets the integer registers. These two signals were never able to revive the test processor after a SEFI event indicating that that the SEFI did not result from upsets in those sections of the processor. The LINT0 signal was observed to pause the operation of the processor when asserted during calibration experiments. The processor continued normal operation after the signal was deactivated. However, this signal was not able to revive the processor after SEFI events in any of the SEFI experiments. All other signals were able to restore the normal operation of the CPU with varying level of success rates. As expected, the signals IRQ5, LINT1/NMI, and RESET# resulted in increasing success rates due to the corresponding increase in their level of severity. For example, IRQ5 is a maskable signal and resulted in recovery in only 27.3% of experiments while the non-maskable LINT1/NMI signal resulted in a success

rate of 66.7%. Similarly, the software and APIC watchdogs resulted in lower success rates as compared to the hardware watchdog because they are dependent on the normal operation of a set of the processor's internal sub-circuits. If one of these internal sub-circuits is affected by the SEFI event, the corresponding watchdog scheme is probable to fail.

5 Conclusions

The results presented here illustrate the ability of the H-Core technique to detect the occurrences of SEFI events in an Intel Pentium III processor and to restore its normal operation without requiring the removal of power supply from the computer system. The H-Core uses a set of control signals with increasing level of severity to coerce the processor to a valid state after detecting a SEFI event. This allows the processor's operation to be restored using the least severe signal necessary, allowing the system to be operational with minimum amount of delay. Proton irradiation experiments performed on a Pentium III processor show that the processor could be recovered from SEFI in every case using the set of signals used. Similar tests are currently in progress on three different commercial processors in addition to the Intel PIII processor. The results of these tests will also be reported at the conference and will be included in the final paper.

Bibliography

- [1] F. Irom, F. Farmanesh, A. Johnston, G. Swift, and D. Millward, "Single-Event Upset in Commercial Silicon-On-Insulator PowerPC Microprocessors," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 3148-3155, December 2002
- [2] G. Swift, F. Farmanesh, S. Guertin, F. Irom, and D. Millward, "Single-Event Upset in the PowerPC750 Microprocessor," 2001
- [3] J. Howard Jr., M. Carts, R. Stattel, C. Rogers, T. Irwin, C. Dunsmore, J. Stattel, C. Rogers, T. Irwin, C. Dunsmore, J. Sciarini, and K. LaBel, "Total Dose and Single Event Effects Testing of the Intel Pentium III (P3) and AMD K7 Microprocessors," *IEEE Radiation Effects Data Workshop*, vol. , no. , pp. 38-47, 16-20 July 2001
- [4] Intel Corporation, "Pentium III Processor for the PGA370 Socket at 500MHz to 1.13GHz: Datasheet Revision B," 2001