

Radiation Hardened 8 Gb NAND Flash Module

Radiation hardened non-volatile memories for space are still confined to EEPROM. There is no flash memory acceptable for use in space due mainly to available flash die being susceptible to radiation single event effects of SEU (Upset) and SEFI (Functional Interrupt and block errors). Bit flips (Upsets) may be tolerable for certain types of data, but if they occur in the processing instructions, functional errors can result in corrupt data or total lock-up of the flash circuit.

The current state-of-the-art 8 Gb product incorporates ground breaking Space Micro radiation mitigation technologies.

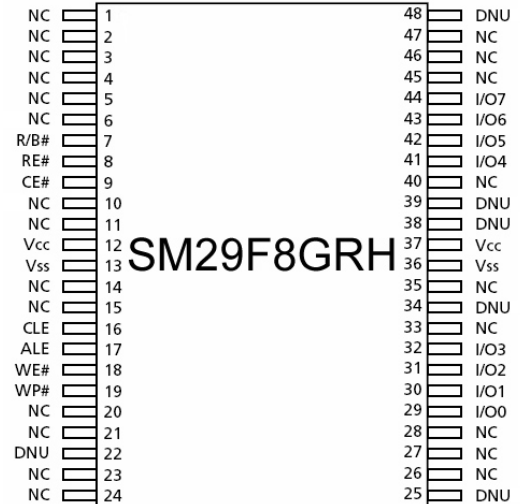
Features for Space Applications

- TID: >100 krad(Si)
- SEL: none >58.7MeV/mg/cm²
- SEU: all single bit errors corrected
- SEFI: no SEFI or block errors

Space Micro has selected an 8 Gb NAND flash device based on radiation testing data. Unprotected, this flash device exhibits SEU and SEFI deficiencies and is rated "Recommended for usage in some NASA / GSFC spaceflight applications but requires extensive mitigation techniques or hard failure recovery mode." Space Micro's 8 Gb flash incorporates patent-pending radiation mitigation technologies, solving the radiation issues seen in the commercial part.

General

- Single 3.3V Power Supply
- Organization
 - Memory Cell (512M+6M)x8 or (256M+3M)x16
 - Data Register: (2K+64) x 8bit
- Automatic Program and Erase
 - Page Program: (2k +64) Byte
 - Block Erase (128k +4k) Byte
- Page Read Operation
 - Page Size: (2k + 64) Byte
 - Random Read: 29us (Max)
 - Serial Access: 25ns (Min.)
 - Command Driven Operation
- Fast Write Cycle Time
 - Page Program time: 200μs (Typical)
 - Block Erase Time: 1.5ms (Typical)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
 - Program/Erase lockout during pwr. transitions
- Reliable CMOS Floating-Gate Technology
 - Endurance: 100K Program/Erase cycles (with 1 bit/512 Byte ECC)
 - Data Retention: 10 years
- Intelligent Copy-Back w/ intern 1-bit / 528B EDC



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Space Micro Radiation Mitigation Technologies Application



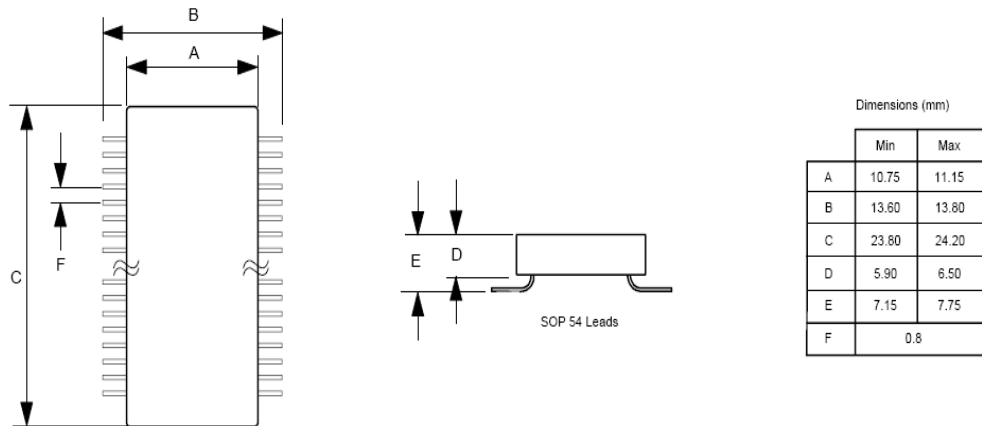
Flash Module Stacking Design

- 5 layer stack
 - 3 flash layers
 - ASIC SEU-SEFI Layer
 - Power control switching layer
 - 20.6 x 13 x 9.45 mm (max)
(commercial Flash IC footprint)

Layer 1	SEU & SEFI Control Logic
Layer 2	Flash 1
Layer 3	Flash 2
Layer 4	Flash 3
Layer 5	Power Control Switch

Package

- 48-pin TSOP or 52-pad LGA, compatible with commercial Flash IC footprint. 11 x 24 mm.



DC Operating Conditions And Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.3	3.6	V
Input high voltage	V _{IH}	0.8 x V _{CC}	-	V _{CC} +0.3	V
Input low voltage, All inputs	V _{IL}	-0.3	-	0.2 x V _{CC}	V
Output high Voltage Level	V _{OH}	0.67 x V _{CC}	-	-	V
Output low voltage Level	V _{OL}	-	-	0.4	V
Operating Current	I _{CC}	-	80	120	mA
Operating Temperature	T	-40	-	+85	C

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _{I/O}	-0.6 to V _{CC} + 0.3 (<4.6V)	V
Storage temperature	T _{STG}	-65 to +150	C

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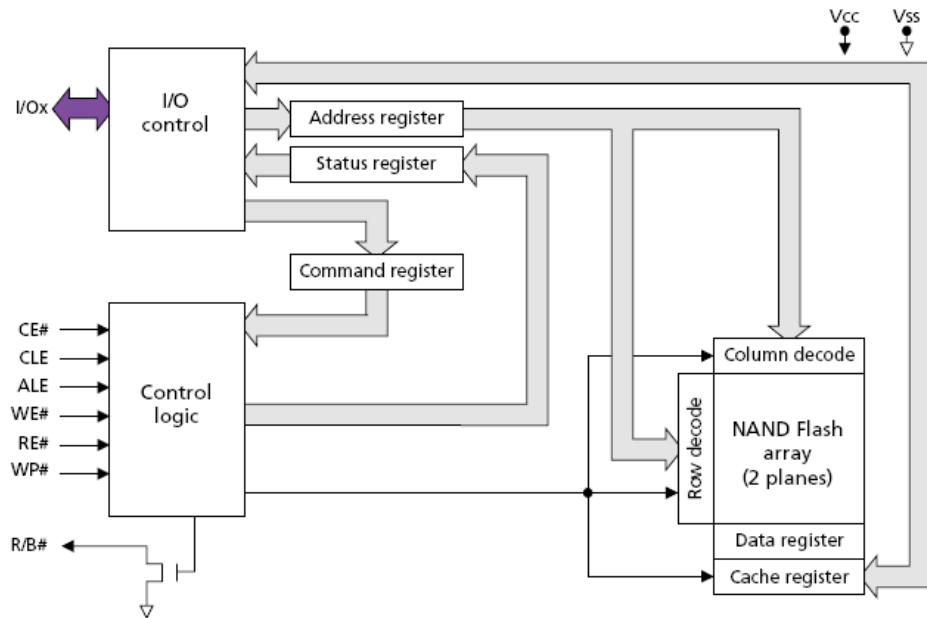
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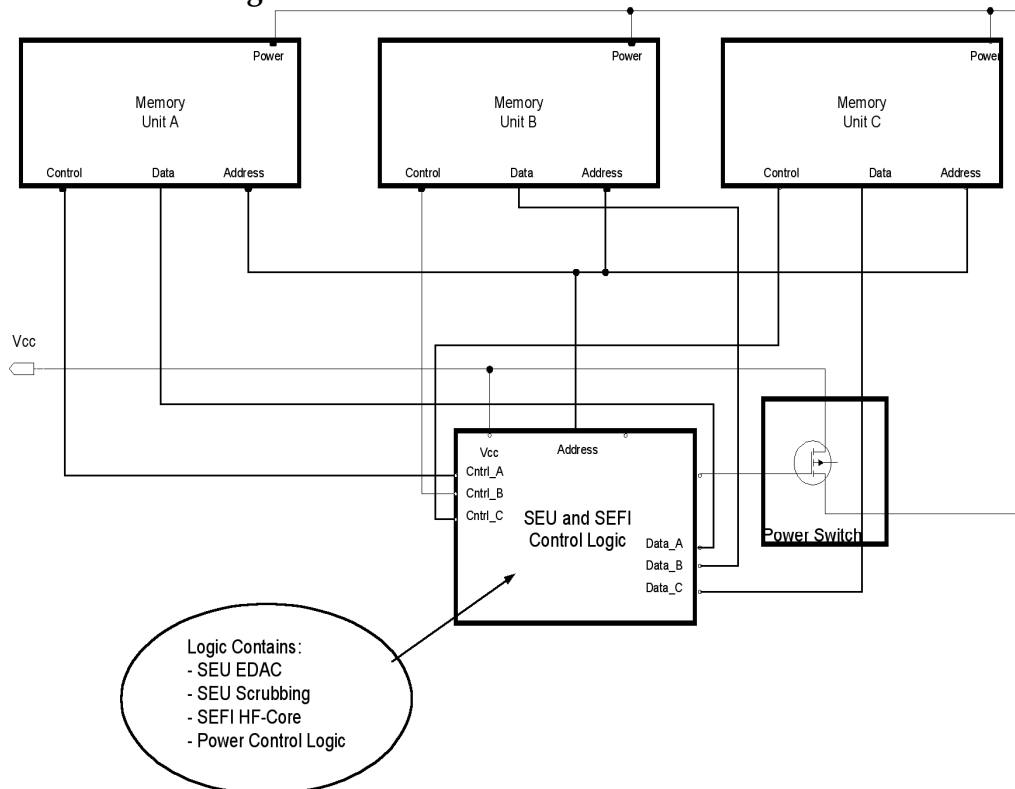


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Flash Die Circuit Design



Flash Module Circuit Design



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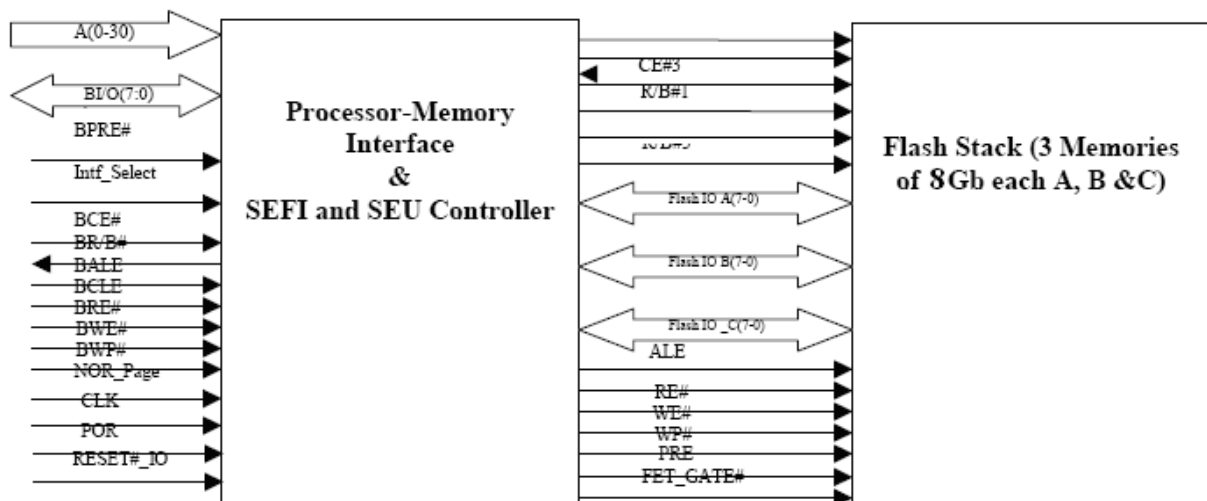
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Pin Description

- BALE - Address Latch Enable from Host. During the time BALE is HIGH, address information is transferred from BI/O[7:0] into the controllers address register upon a LOW to HIGH transition on BWE#. When address information is not being loaded, the BALE pin should be driven LOW.
- BCE# - Chip Enable from Host. Gates transfers between the host system and the controller.
- BCLE - Command Latch Enable from Host. When BCLE is HIGH, information is transferred from BI/O[7:0] to the controllers command register on the rising edge of BWE#. When command information is not being loaded, the BCLE pin should be driven LOW.
- BRE# - Read Enable from Host. Gates transfers from the Controller to the host system.
- BWE# - Write Enable from Host. Gates transfers from the host system to the controller.
- BWP# - Write Protect from Host. Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when the BWP# pin is LOW.
- BI/O[7:0] – I/O Line. The bidirectional BI/O pins transfer address, data, and instruction information between the host and the controller. Data is output only during READ operations; at other times the BI/O pins are inputs.
- BR/B# - Ready/Busy from controller. The pin is used to indicate when the controller is processing a PROGRAM or ERASE operation. The pin is also used during a READ operation to indicate when data is being transferred from the memories into the controllers serial data register. Once these operations have completed, BR/B# returns to the high-impedance state.
- EDAC On – Determines if the chip will enable the EDAC.



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Product Organization

The SMI-FLASH-8G-29F8G is an 8 Gb memory device that consists of 2 planes per die. Each plane consists of 2,048 blocks. Each block is subdivided into 64 programmable pages. Each page consists of 4,314 bytes. The pages are further subdivided into a 4,096-byte data storage region with a separate 218-byte area. The 218-byte area is typically used for error management functions.

The SMI-FLASH-8G-29F8G has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE to low while CE is low. Those are latched on the rising edge of WE. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The physical space requires 30 addresses, thereby requiring five cycles for addressing: 2 cycles of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register.

List of Commands

Operation	Cycle 1	Cycle 2
Normal Page Read	00h	30h
Random Data Read	05h	E0h
Read Test Mode	00h	30h
Block Erase	60h	D0h
Normal Program Page	80h	10h
Random Data Input	85h	-
Write Test Mode	80h	10h
Reset	FFh	

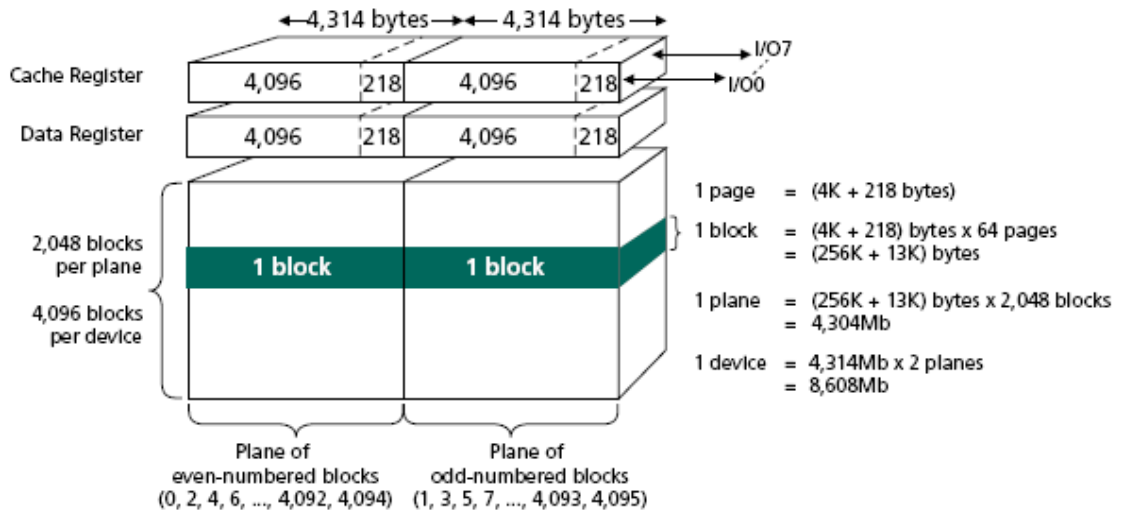
List of commands for NAND Interface

Apart from these instructions, the following WRITE PROTECT operations can also be performed:

- Erase Disable (BWP# is low)
- Program Disable (BWP# is low)
- Erase Enable (BWP# is high)
- Program Enable (BWP# is low)

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Flash Array Organization



Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7	BA6 ³	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L		H	X	Read mode	Command input
L	H	L		H	X		Address input
H	L	L		H	H	Write mode	Command input
L	H	L		H	H		Address input
L	L	L		H	H	Data input	
L	L	L	H		X	Sequential read and data output	
X	X	X	H	H	X	During read (busy)	
X	X	X	X	X	H	During program (busy)	
X	X	X	X	X	H	During erase (busy)	
X	X	X	X	X	L	Write protect	
X	X	H	X	X	0V/Vcc ¹	Standby	

- Notes: 1. WP# should be biased to CMOS HIGH or LOW for standby.
 2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

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Program Erase Characteristics

Symbol	Parameter	Typ	Max	Unit	Notes
NOP	Number of partial-page programs	-	4	cycles	1
^t BERS	BLOCK ERASE operation time	0.7	3	ms	
^t CBSY	Busy time for CACHE PROGRAM operation	20	700	μs	2
^t DBSY	Dummy busy time for two-plane operations	0.5	1	μs	
^t FEAT	Busy time for SET FEATURES and GET FEATURES operations	-	1	μs	
^t LPROG	LAST PAGE PROGRAM operation time	-	-	-	3
^t OBSY	Busy time for OTP DATA PROGRAM operation if OTP is protected	-	25	μs	
^t PROG	PROGRAM PAGE operation time	250	700	μs	

- Notes: 1. Four total to the same page.
 2. ^tCBSY MAX time depends on timing between internal program completion and data in.
 3. ^tLPROG = ^tPROG (last page) + ^tPROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min ¹	Max ¹	Unit	Notes
ALE to data start	^t ADL	70	-	ns	2
ALE hold time	^t ALH	5	-	ns	
ALE setup time	^t ALS	10	-	ns	
CE# hold time	^t CH	5	-	ns	
CLE hold time	^t CLH	5	-	ns	
CLE setup time	^t CLS	10	-	ns	
CE# setup time	^t CS	15	-	ns	
Data hold time	^t DH	5	-	ns	
Data setup time	^t DS	7	-	ns	
WRITE cycle time	^t WC	20	-	ns	
WE# pulse width HIGH	^t WH	7	-	ns	
WE# pulse width	^t WP	10	-	ns	
WP# setup time	^t WW	30	-	ns	

- Notes: 1. Operating-mode timings meet ONFI timing mode 5 parameters.
 2. Timing for ^tADL begins in the ADDRESS cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.

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AC Timing Characteristics for Operation

Parameter	Symbol	Min ¹	Max ¹	Unit	Notes
ALE to RE# delay	^t AR	10	-	ns	
Change column setup time	^t CCS	70	-	ns	
CE# access time	^t CEA	-	25	ns	
CE# HIGH to output High-Z	^t CHZ	-	30	ns	2
CLE to RE# delay	^t CLR	10	-	ns	
CE# HIGH to output hold	^t COH	15	-	ns	
Cache busy in page read cache mode (first 31h)	^t DCBSYR1	-	5	µs	
Cache busy in page read cache mode (next 31h and 3Fh)	^t DCBSYR2	^t DCBSYR1	25	µs	
Output High-Z to RE# LOW	^t IR	0	-	ns	
Data transfer from Flash array to data register	^t R	-	25	µs	
READ cycle time	^t RC	25	-	ns	
RE# access time	^t REA	-	20	ns	3
RE# HIGH hold time	^t REH	7	-	ns	3
RE# HIGH to output hold	^t RHOH	15	-	ns	3
RE# HIGH to WE# LOW	^t RHW	100	-	-	
RE# HIGH to output High-Z	^t RHZ	-	100	ns	2, 3
RE# LOW to output hold	^t RLOH	5	-	ns	
RE# pulse width	^t RP	10	-	ns	
Ready to RE# LOW	^t RR	20	-	ns	
Reset time (READ/PROGRAM/ERASE)	^t RST	-	5/10/500	µs	4
WE# HIGH to busy	^t WB	-	100	ns	5
WE# HIGH to RE# LOW	^t WHR	60	-	ns	

- Notes:
1. Operating-mode timings meet ONFI timing mode 4 parameters.
 2. Transition is measured $\pm 200\text{mV}$ from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
 3. AC characteristics may need to be relaxed if I/O drive strength is not set to "full." See Table 14 on page 50 for additional details.
 4. If RESET (FFh) command is loaded at ready state, the device goes busy for maximum 5µs.
 5. Do not issue a new command during ^tWB, even if R/B# is ready.

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