**µSDR-C™ Software Defined Radio**

**µSDR-C Dimensions:** 10 cm x 10 cm x 8 cm

**KEY FEATURES**

- Small Form Factor Software Defined Radio
- Radiation Hardened
- Suitable for LEO, GEO
- FPGA Reconfigurable Resources, Transceiver Chip
- Base µSDR-C using 2 Board Set (DPS + RF Transceiver) provides 150 MHz to 6 GHz operation
- Optional Up/Down Converter Board with Low Noise Amplifier (LNA), Power Amplifier (PA) available
- Interfaced with KG-250 NSA Type 1 Cryptographic Unit (Option)

**BLOCK DIAGRAM**

- **µSDR-C**
  - 512MB DDR3L
  - OSC 33.33 MHz
  - PROCESSING SYSTEM: Dual core ARM Cortex-A9
  - 3 FLASH Chips Gigabyte
  - WATCHDOG, FLASH CTRL, 10 MHz PLL
  - BACKPLANE CONNECTOR 300 Pin Searay
  - 1GB DDR3L PL
  - PROGRAMMABLE LOGIC 125k CELLS, 9.5 Mb RAM, 593GMACs
  - RF TRANSCEIVER
  - OSC 40 MHz VCXO

- **CSP Processor** (Digital Software Defined Radio)
  - PROCESSING SYSTEM: Dual core ARM Cortex-A9
  - 3 FLASH Chips Gigabyte
  - WATCHDOG, FLASH CTRL, 10 MHz PLL
  - BACKPLANE CONNECTOR 300 Pin Searay
  - 1GB DDR3L PL
  - PROGRAMMABLE LOGIC 125k CELLS, 9.5 Mb RAM, 593GMACs
  - RF TRANSCEIVER
  - OSC 40 MHz VCXO

- **Personality Card**
  - RF DAC
  - CAN
  - Ext Clk
  - 10MHz Ref
  - SGMII
  - Boot Cfg
  - JTAG

- **Digital Signal Processor Board**

- **RF Transceiver Board**

- **Up/Down Converter Board (Optional)**

**µSDR-C Specifications**

- **Dimensions:** 10 cm x 10 cm x 8 cm
- **Operational Bandwidth:** 150 MHz to 6 GHz
- **Input Band:** 2025-2120 MHz
- **Output Band:** 8.0-8.4 GHz
- **Output Power:** +33dBm
- **Power Amplifier:** 1W-10W SSPA

**µSDR-C Features**

- Small Form Factor
- Radiation Hardened
- Suitable for LEO, GEO
- FPGA Reconfigurable Resources
- Interfaced with KG-250 NSA Type 1 Cryptographic Unit

**Contact Information**

15378 Avenue of Science, Suite 200, San Diego, CA 92128
858.332.0700 | sales@spacemicro.com | www.spacemicro.com
# µSDR-C™ Software Defined Radio

## Transceiver Features

**Carrier Frequency**  
150 MHz — 6 GHz

**Tunable Channel Bandwidth**  
<200kHz to 56 MHz

**Data rate**  
1 kbps to 42 Mbps using Higher Modulation Codes

**RF Output Power**  
User configurable: 6.5 dBm to 8 dBm from RF Transceiver  
Optional Power Amplifier: 1 to 10 Watts RF Power

**LO step size**  
< 2.4 Hz

**Encoding**  
CCSDS ReedSolomon(255,223), Interleave=5, CONVO (7,1/2), LDPC and User Provided Options Available

**Modulation**  
BPSK, OQPSK, 8PSK, 16APSK, FSK

**ADC/DAC**  
12-bits, Optimized Sample Rate of 30.72 Msps  
Optional Sample Rate up to 61.44 Msps

## Receiver Section

**Noise Figure**  
UHF: < 2.5 dB  
S-band: 3 dB  
C-band: 3.8 dB

**Dynamic Range**  
Threshold (Minimum) -21 dBm (Maximum)

**Sensitivity**  
-109 dBm (Maximum)

**100 kbps, 16-ary FSK, 1E-6 BER Range**  
Dependent on RF Power Output and Antenna Selection

**Power—Receiver Only**  
4 W (Typical)  
5 W (Maximum)  
Transmitter Power Determined by Required Output Power Needed

## General Specifications

- Size: 10 x 10 x 5 cm (2 Board Base Model); 10 x 10 x 8 cm (3 Board Model)
- Weight: <0.6 kg (2 Board Model); < 0.75 kg (3 Board Model)
- Operating Temperature: -30° C to +60° C (contact factory for other temperature ranges)
- Storage Temperature: 50°C to + 85°C
- Vacuum Environment: 10E-5 Torr
- Power consumption: 8 Watt
- Radiation
  - 30, 50 and 100 krad models available
  - No SEL <70 MeV/mg/cm²
  - No unrecoverable SEFI
µSDR-C™ Software Defined Radio

I/O AND INTERFACES

Telemetry Outputs
- Received Signal Strength Indicator (RSSI)
- Automatic Gain Control (AGC)
- Carrier and Demod Lock
- Frequency and Time Offset
- Critical Voltages
- Critical Temperatures

Programmable I/O
- 14 User Programmable I/O Pins on µD 15-pin Header
- Differential Routed Pairs on 2.5 V Bank
- LVDS25 or LVCMOS25 Standards
- Bus Routed

Standards Available on µD 15-pin connector
- Standards available in Zynq EMIO
- SPI
- UART
- I2C
- CAN (Phy not on backplane)
- No Ethernet
- SpaceWire (tested to 100 Mbps) Core Provided
- EtherWire

Telemetry Interface
User Defined

INPUT VOLTAGE

Maximum Input Power
2.5 dBm to the Transceiver
Slice Available for Signal Conditioning of Power Prior to Entering the Transceiver Chip

POWER CONSUMPTION

<table>
<thead>
<tr>
<th>Element</th>
<th>Tx &amp; Rx Power</th>
<th>Tx Power</th>
<th>Rx Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Processing</td>
<td>1.8</td>
<td>1.3</td>
<td>1.3</td>
</tr>
<tr>
<td>Agile Converter</td>
<td>2.1</td>
<td>1.3</td>
<td>1.3</td>
</tr>
<tr>
<td>Up convert</td>
<td>1.6</td>
<td>1.6</td>
<td>0</td>
</tr>
<tr>
<td>Down convert</td>
<td>1.6</td>
<td>0</td>
<td>1.6</td>
</tr>
<tr>
<td>Freq Synthesis</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Power Amp (2W)</td>
<td>6.6</td>
<td>6.6</td>
<td>0</td>
</tr>
<tr>
<td>LNA</td>
<td>0.3</td>
<td>0</td>
<td>0.3</td>
</tr>
<tr>
<td>Misc</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>TOTAL</td>
<td>15.5</td>
<td>12.3</td>
<td>6</td>
</tr>
<tr>
<td>Option: +28V DC-DC Conversion</td>
<td>25%</td>
<td>25%</td>
<td>25%</td>
</tr>
</tbody>
</table>